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APPLICATION FOR PATENT

FOR INVENTION OF

APPARATUS AND METHOD FOR SIGNAL TRANSMISSION

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APPARATUS AND METHOD FOR SIGNAL TRANSMISSION

1. Field of the invention.

The present invention is related to the field of electronic devices, and more specifically to devices and circuits configured as signal transmission gates and methods for transmitting signals.

2. Background.

In electronic circuits, certain classes of signals often have a voltage or a current whose value encodes information. The information can be a measured value of a quantity, a number, etc.

Such signals are used within the circuit for processing the encoded information. Processing, however, attenuates the strength of such signals, which renders them less reliable for further processing.

Transmission gates are electronic circuits that are used to control when such signals are to be transmitted within the circuit. Transmission gates receive the signal as an input, and generate the restored signal as an output, when it is desired. In so doing, a transmission gate restores such signals to their original strength, so that they can be used for further processing.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will become more readily apparent from the Detailed Description, which proceeds with reference to the drawings, in which:

FIGURE 1 is a schematic diagram of a transmission gate;

FIGURE 2 is a table of values for illustrating an operation of the circuit of FIGURE 1;

FIGURE 3 is a schematic diagram of another transmission gate;

FIGURE 4 is a schematic diagram of yet another transmission gate;

FIGURE 5 is a timing diagram illustrating a time variation in the voltage of a capacitor in FIGURE 4;

FIGURE 6 is a schematic diagram illustrating a signal transmission gate according to an embodiment of the invention;

FIGURE 7 is a timing diagram illustrating that a substantially constant voltage above an input voltage is applied at the gate of a switch is in the diagram of FIGURE 6;

FIGURE 8 is a schematic diagram illustrating an embodiment of a constant-voltage boosting circuit for the gate of FIGURE 6;

FIGURE 9 is a schematic diagram of the circuit of FIGURE 8, as further modified to correct also for threshold voltage variation based on an input signal value;

FIGURE 10 is a schematic diagram illustrating a multiplexer made from two gates;

FIGURE 11 is a diagram illustrating one more transmission gate; and

FIGURE 12 is a block diagram illustrating a method according to the invention.

DETAILED DESCRIPTION

The present invention is now described. While it is disclosed in its preferred form, the specific embodiments of the invention as disclosed herein and illustrated in the drawings are not to be considered in a limiting sense. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Indeed, it should be readily apparent in view of the present description that the invention may be modified in numerous ways. Among other things, the present invention may be embodied as devices, methods, and so on. Accordingly, the present invention may take the form of an entirely hardware embodiment, an entirely method embodiment or an embodiment combining method and hardware aspects. The following detailed description is, therefore, not to be taken in a limiting sense.

Throughout the specification, the meaning of "a," "an," and "the" may also include plural references. The meaning of "in" includes "in" and "on."

Generally, the invention is directed to signal transmission gates, and methods of transmitting signals. The invention is advantageously applied for digital and analog signals. Briefly, a signal transmission gate includes a switch such as a transistor. The switch includes a gate terminal adapted to receive a control voltage, and a source terminal

and a drain terminal. One of the source and drain terminals is adapted to receive an input signal, and the output signal is produced on the other terminal. A constant-voltage boosting circuit generates the control voltage such that it has a substantially constant value above a voltage of the input signal. In one embodiment, the constant-voltage boosting circuit is coupled between the source terminal and the gate terminal, and generates a substantially constant voltage difference. In one implementation, a component is employed that exhibits a characteristic voltage behavior, such as a diode, for generating the substantially constant voltage difference.

FIGURE 1 is a schematic of transmission gate 100. Gate 100 is made from NMOS transistor 110 and PMOS transistor 120, coupled in parallel with joined terminals as shown. Transistors 110 and 120 are controlled respectively by voltages V_{GN}, V_{GP}, which are applied to their gates. Output signal V_{OUT} is generated in response to receiving input signal V_{IN}.

FIGURE 2 is a table showing an example of how gate 100 of FIGURE 1 may be controlled by individually controlling transistors 110 and 120. For the examples of FIGURE 2, voltages V_{GN} and V_{GP} are the logical inverse of each other. In other words, when one of them is zero ("ground", or "GND"), the other one is placed at the full value of a supply voltage V_{DD}.

As can be seen in FIGURE 2, gate 100 may be turned on for a signal transmission operation. This way, the generated output voltage V_{OUT} equals substantially input voltage V_{IN}. Alternately, gate 100 may be turned off. In that instance, there is no output signal being generated, regardless of the value of input voltage V_{IN}.

In gate 100, when input voltage V_{IN} is near the value of supply voltage V_{DD}, NMOS transistor 110 does not conduct. And when input voltage V_{IN} is near GND, it is PMOS transistor 120 that does not conduct.

A challenge is that, when gate 100 is turned on, output voltage V_{OUT} does not equal input voltage V_{IN} for values of V_{IN} that are about midrange between GND and V_{DD}, because of the higher on resistance at that range, which results from the fact that neither transistor is fully turned on. In other words, there is reduced signal integrity in the midrange. That occurs because the gate-to-source potential V_{GS} needs to be larger than a

threshold voltage of a corresponding transistor. While this occurs in the ends of the range for at least one of transistors 110, 120, it occurs for neither in the midrange.

Further, there are constraints in the size of transistors 110, 120. Making them larger reduces the on-resistance, but beyond some point their parasitic capacitance becomes too large.

FIGURE 3 is a schematic of transmission gate 300. Gate 300 is made from NMOS transistor 310 and PMOS transistor 320, coupled similarly as transistors 110, 120 of gate 100 respectively. In addition, voltage boosting circuit 340 is coupled between supply voltage V_{DD} and the gate of NMOS transistor 310.

Circuit 340 generates a voltage difference V_{BOOST}, and may be implemented by a circuit such as a charge pump and/or a capacitor. The value of V_{BOOST} may be constant with time, and in any way does not adapt when the value of input voltage V_{IN} changes. Circuit 340 has the effect of increasing voltage V_{GN} applied to the gate of NMOS transistor 310 above supply voltage V_{DD}. The increase is by an amount V_{BOOST}. In other words, V_{GN} substantially equals $V_{DD} + V_{BOOST}$. This lowers the on resistance of NMOS transistor 310, at the expense of an increased gate-to-source voltage when input voltage V_{IN} is close to GND.

In the application of FIGURE 3, a boosting voltage was applied to NMOS transistor 310, but not to PMOS transistor 320. Transmission gate 300 may be further implemented by applying a boost to PMOS transistor 320, such as a negative boost.

FIGURE 4 is a schematic of transmission gate 400 that uses NMOS transistor 410. Further, capacitor C_B 430 is coupled to switch 440.

In terms of operation, when switch 440 is in an OFF position, capacitor C_B 430 is charged to a large value, such as that of supply voltage V_{DD}, or other value. When switch 440 is in an ON position, capacitor C_B 430 maintains the gate of NMOS transistor 410 at a value V_{GN} that is higher than that of input voltage V_{IN} by the capacitor voltage V_{CB}.

FIGURE 5 is a timing diagram showing graphed evolution 510 of capacitor voltage V_{CB}. It is not constant with time; as time passes, capacitor C_B 430 discharges, and its voltage decreases due to leakage. Because of the leakage, gate 400 must be switched off regularly, to recharge capacitor C_B from supply voltage V_{DD}. Accordingly, the arrangement works when gate 400 is switched off and back on repeatedly.

For gates 300 and 400, an overdrive voltage may occur at the gates of NMOS transistors 310, 410 respectively. The overdrive voltage is the value of gate voltage V_{GN}, which is above the value of supply voltage V_{DD}. The overdrive voltage needs to be larger than threshold voltage V_{TH}, for NMOS transistors 310, 410 to pass substantially all input signal levels. This overdrive voltage, however, can produce stress in the materials, which may damage the device. In the case of gate 300, some overdrive voltage is applied continuously by circuit 340, albeit by a controlled amount V_{BOOST}. In the case of gate 400, an overdrive voltage is applied intermittently, depending on input voltage V_{IN}. But when the latter approaches a value of supply voltage V_{DD}, the overdrive voltage itself can be as high as V_{DD}.

FIGURE 6 illustrates transmission circuit 600 made according to the invention, which may also be called a transmission gate. Circuit 600 includes input node 612 for receiving input signal V_{IN}, and output node 614 for generating output signal V_{OUT} from input signal V_{IN}. Input signal V_{IN} is therefore transmitted through circuit 600. Transmission switch 610 is coupled between input node 612 and output node 614. Transmission switch 610 further has control terminal 616, on which a control voltage V_{GN} is applied. Transmission switch 610 is controlled by the control voltage.

Transmission switch 610 may be implemented in any number of ways. One such way is, as shown in FIGURE 6, with a switched device such as an NMOS transistor, which is also known as a main transistor. Switch 610 includes a gate terminal coupled to control terminal 616, and adapted to receive control voltage V_{GN}. The switch also includes a source terminal and a drain terminal. One of them is coupled with input node 612, and is adapted to receive input signal V_{IN}. The other one is coupled with output node 614, and adapted to produce on it output signal V_{OUT}.

Since switch 610 is an NMOS, the source terminal may be coupled with input node 612, and the drain terminal may be coupled with output node 614, as would be conventional. If switch 610 instead were a PMOS, then the boost voltage would have to be negative in the ON condition.

In circuit 600, constant-voltage boosting circuit 620 maintains the control voltage V_{GN} at a substantially constant value above a voltage of the input signal V_{IN}. In other

words, control voltage V_{GN} varies, but it does that in substantial unison with input signal V_{IN}.

Boosting circuit 620 may be implemented in any number of ways. In the embodiment of FIGURE 6, boosting circuit 620 is coupled between input node 612 and gate terminal 616. Further, it generates boosted voltage V_{CV}, and maintains it substantially constant. This way, control voltage V_{GN} is maintained at a value substantially equal to the voltage of input signal V_{IN} plus that of boosted voltage V_{CV}.

FIGURE 7 is a timing diagram showing graphed evolution 710 for boosted voltage V_{CV}. As can be seen, boosted voltage V_{CV} remains substantially constant, and is applied substantially constantly. Further the invention accomplishes this without requiring gate 610 to be switched on and off, as was seen in FIGURE 5 for the operation of gate 400 of FIGURE 4.

Evolution 710 remains substantially constant at least for a constant input signal V_{IN}. As will be seen later, it may change based on the level of input signal V_{IN} due to a body effect that affects a threshold voltage V_{TH}, and further the body effect may be compensated.

Returning to FIGURE 6, in some embodiments of the invention transmission switch 610 exhibits a characteristic behavior, which changes depending on a value of input signal V_{IN}. For example, in FIGURE 6 transmission switch 610 includes a main NMOS transistor. The characteristic behavior can be that a threshold voltage of the main NMOS transistor changes depending on the input signal value. In that case, graph 710 in FIGURE 7 should be interpreted as being substantially constant for a constant input signal V_{IN}.

In some of these embodiments, constant-voltage boosting circuit 620 maintains the control voltage at a value above the input signal voltage that is further adjusted. Adjustment is so as to substantially compensate for the characteristic behavior of the transmission switch. An example of that will be described later in this document, with respect to FIGURE 9.

It will be appreciated that transmission gate 600 of FIGURE 6 is able to operate continuously, while resulting in reduced overdrive voltage stress. Indeed such occurs, but not at the critical junctions, i.e. between any two of the gate, source and drain.

Moreover, transmission gate 600 may advantageously be implemented with a relatively small transistor component size, which can reduce parasitic capacitances. This enables gate 600 to allow to pass signals that are changing very quickly, e.g. at 1.6 GHz and higher. Further, since the transistor component size can be relatively small, the leakage current can also be relatively small if transmission gate 600 is OFF. And if it is ON, the resistance can be both low and relatively stable, which can yield high output signal integrity, even at that high speed.

One embodiment of boosting circuit 620 includes a component exhibiting a characteristic voltage behavior. The component may be, for example, a diode, a MOS transistor, a MOS transistor configured as a diode, etc. The component may include a junction between two dissimilar materials, in which case the characteristic voltage behavior is a voltage drop obtained across the junction upon energizing it. This characteristic voltage behavior may be advantageously exploited according to the invention, for generating a V_{CV} as substantially constant with time as is shown in FIGURE 7.

FIGURE 8 is a schematic of exemplary circuit 800 that includes transmission switch 610 previously described with reference to FIGURE 6. Constant-voltage boosting circuit 820 is one of many possible embodiments of implementing boosting circuit 620 of FIGURE 6.

In the embodiment shown in FIGURE 8, boosting circuit 820 includes PMOS transistor 830 and PMOS transistor 840, which are sometimes called control transistors. Control PMOS transistor 840 has a gate coupled to receive input signal V_{IN}. Transistor 830 exhibits a characteristic voltage drop $V_{GS,P1}$, while transistor 840 exhibits a characteristic voltage drop $V_{GS,P2}$. Together, these characteristic voltage drops $V_{GS,P1}$, $V_{GS,P2}$ are combined to maintain the voltage difference of boosted voltage V_{CV} at a substantially constant level, as per the invention.

Furthermore, the connection of PMOS transistor 840 allows input signal V_{IN} to set the V_{GS} of transmission switch 610, without adding a DC load on input signal V_{IN}. Note that this is accomplished in a simple fashion, which avoids the use of an amplifier. This renders the present invention able to work concurrently at low power and with high bandwidth.

First current source 850 is adapted to drive a bias current I_{BIAS} through transistors 830, 840 to energize them. This generates the characteristic voltage drops $V_{GS,P1}$, $V_{GS,P2}$, and thus also boosted voltage V_{CV}. Second current source 855 and current mirror 860 control first current source 850. Current mirror 860 thus forces the bias current I_{BIAS} of current source 850 to be set according to a current I_{SET} of second current source 855. As a design point, then, I_{SET} is set to control the desired value of I_{BIAS}.

It is preferred that transistor 880 be provided, configured as a diode and coupled to ground for draining the current of current source 850. Transistor 880 has a voltage drop, and thus prevents the application of too high a voltage across the source and drain of transistor 840.

Preboosting node 865 is maintained at a voltage V_{PB}, which may be maintained constant. Preboosting circuit 870 boosts voltage V_{PB} of preboosting node 865. For example, preboosting circuit 870 may be coupled to a supply voltage V_{DD}, and thus raise voltage V_{PB} above the value of supply voltage V_{DD}. Preboosting circuit 870 may be made in any way known in the art. For example, it may be made by a charge pump.

In the embodiment of FIGURE 8, there is at least one electrical component between preboosting node 865 and the control terminal of transmission switch 610. In this instance, this electrical component is current source 850. This ensures that control voltage V_{GN} does not reach unnecessarily high values, and eases the task of regulating the voltage difference of boosted voltage V_{CV}.

As also described above, in some embodiments of the invention, the constant-voltage boosting circuit further adjusts the control voltage depending on the value of input signal V_{IN}, to allow for the fact that the threshold voltage itself may change depending on the value of input signal V_{IN}. An example of that is described below.

FIGURE 9 is a schematic of circuit 900 that is largely similar to circuit 800 of FIGURE 8. The difference is found in that constant-voltage boosting circuit 920 is somewhat different from constant-voltage boosting circuit 820. The difference is that NMOS control transistor 930 is provided, instead of PMOS control transistor 830. Transistor 930 exhibits a characteristic voltage drop $V_{GS,N}$. Together with voltage drop $V_{GS,P2}$ of transistor 840, these characteristic voltage drops are combined to generate a boosted voltage V_{CV}.

Boosted voltage V_{CV} remains substantially constant, as per the invention, except it changes somewhat depending on the value of input signal V_{IN}. Regardless, control NMOS transistor 930 is arranged so that a behavior of its threshold voltage substantially cancels the characteristic behavior of the threshold voltage of transistor 610, as input signal V_{IN} changes. Indeed, as input signal V_{IN} changes, the threshold voltage of transistor 930 changes in substantial unison with the threshold voltage of transistor 610, and the body effect of the two transistors remains the same. As such, constant-voltage boosting circuit 920 further adjusts boosted voltage V_{CV} so as to substantially compensate for the characteristic behavior of transistor 610.

Furthermore, it is preferred that NMOS transistor 930 be provided as a diode as shown, and matches transistor 610. This way the on-resistance varies less over temperature and process.

FIGURE 10 is a schematic of multiplexer 1000 that includes two transmission circuits 1010, 1020. Each transmission circuit 1010, 1020 may be arranged substantially similarly to transmission circuit 600 of FIGURE 6. Their output nodes are coupled.

In operation, the input node of transmission circuit 1010 receives input voltage V_{IN}. Input voltage V_{IN} may be received from the chip that circuit 1000 is implemented on, or from off-chip. Additionally, the input node of transmission circuit 1020 receives a known calibration voltage V_{CAL}. Calibration voltage V_{CAL} may change by stepping through successive voltages, to assist in calibration. In one embodiment, the successive voltages differ by a fixed amount.

Transmission circuit 1010 may be turned off, while transmission circuit 1020 may be used for calibration. Then transmission circuit 1020 may be turned off, while transmission circuit 1010 may be used for transmitting signals with high integrity and low leakage current.

FIGURE 11 is a schematic diagram of exemplary transmission circuit 1100 that includes components arranged in substantially the same manner as those components shown in circuit 600. For example, transmission switch 610 and constant-voltage boosting circuit 620 are arranged to produce a first output voltage V_{OUT1} at output node 1140. In addition, second transmission switch 1120 is coupled between input node 1130

and second output node 1150. Second output voltage V_{OUT2} is produced at second output node 1150.

A single transmission circuit 1100 can be used to output a number of calibration voltages, of the type of calibration voltages received by circuit 1020 of FIGURE 10. The arrangement of FIGURE 11 can improve noise isolation between different output channels.

Referring now to FIGURE 12, block diagram 1200 illustrates a method according to an embodiment of the invention. The method of diagram 1200 may also be practiced by different embodiments, including but not limited to circuit 600 of FIGURE 6, circuit 1000 of FIGURE 10, and circuit 1100 of FIGURE 11.

At block 1205, the process of the main operation of a transmission circuit occurs, in connection with other operations at other blocks. An output voltage is generated from an input voltage, as controlled by a control voltage that remains at a substantially fixed level above the input voltage. In some embodiments, the other operations are concurrent and/or optional.

At block 1210, the process receives an input voltage, and provides it at least for the main operation at block 1205. The input voltage may be received at a transmission gate.

Also, at block 1220, the process optionally pumps charge to a preboosting node to generate a preboosted voltage, and optionally provides it at least to the operation of block 1205. Additionally at block 1230, the preboosted voltage may optionally be regulated. This regulation enables the generation of a control voltage that has a substantially constant value above the input voltage. The process at block 1230 may be performed in cooperation with the process at block 1220.

At block 1240, an output voltage is generated from the input voltage received at block 1210. This is performed, for example, at an output node of a transmission gate. At block 1250, which cooperates with block 1205, the control voltage regulated at block 1230 is applied to control the generating of the output voltage at block 1240.

Numerous details have been set forth in this description, which is to be taken as a whole, to provide a more thorough understanding of the invention. In other instances,

well-known features have not been described in detail, so as to not obscure unnecessarily the invention.

The invention includes combinations and subcombinations of the various elements, features, functions and/or properties disclosed herein. The following claims define certain combinations and subcombinations, which are regarded as novel and non-obvious. Additional claims for other combinations and subcombinations of features, functions, elements and/or properties may be presented in this or a related document.